UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,184	02/13/2004	Jonathan R. Fales	BUR920040037US1	2183

24241 7590 06/28/2006

IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
1000 RIVER STREET
972 E
ESSEX JUNCTION, VT 05452

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,184	FALES ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,9 and 10* is/are rejected.

7)☒ Claim(s) *2-5,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/13/04 7/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10 are presented for examination.

Allowable Subject Matter

Claims 2-4, 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 would be allowable over the prior arts when the formal issues are resolved.

The following is a statement of reasons for the indication of allowable subject matter: The present invention pertains to a method and circuit which allow for high speed testing of embedded memories. The claimed invention (claim 5) recites "A command multiplier that generates multiple sets of command, address, and data inputs (CAD) from a seed CAD set having a plurality of bits provided at a low frequency to a memory system at a high frequency, comprising: c directive registers corresponding to c seed CAD bits, each register having one or more directive bits; a logic unit (LU) taking as an input the i th bit of the seed CAD, all of the bits from the i th directive register, and a binary-encoded time interval, m; and a multiplexer for time-multiplexing n generated CAD sets to the memory system at a frequency n times greater than the frequency at which the seed CAD set is received"

The prior arts fail to teach the above combination of elements such as "c directive registers corresponding to c seed CAD bits, each register having one or more directive

bits; a logic unit (LU) taking as an input the i th bit of the seed CAD, all of the bits from the i th directive register, and a binary-encoded time interval, m;" As such, modification of the prior art of record can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the limitations set forth in claim 5 of the present application.

Claim Objections

Claim 5 is objected to because of the following informalities: The independent claim must end in a period. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 9, the phrase "ending the seed CAD set from the BIST to a logic block to generate n CAD sets;", is unclear. IT is unclear to the examiner why at this point in testing the seed would be ended. As this is not clear in the Specification why the seed CAD would be ended at this point or how the test would be able to continue from

this point this claim will not be further considered with respect to prior art until clarification is made.

Claim 10 is dependent on independent claim 9 and therefore inherits the 35 U.S.C. 112, second paragraph issues of the independent claim ans as such will not be further considered on its merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims I and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. U.S. Patent No. 6,647,524.

As per claim 1, Huang et al teach the claimed command multiplier that generates sets of command, address, and data inputs (CAD) from a seed set having a plurality of bits provided at a low frequency by a BIST, to an embedded memory at a high

frequency, comprising: a directive register (delay buffer column 4 lines 19-25); a logic unit (producer, column 3 lines 64-67, packet builder column 4 lines 1-11, compactor column 4 lines 26-29); and a multiplexer for time-multiplexing n generated CAD sets to the memory system at a frequency n times greater than the frequency at which the seed CAD set is received (column 4 lines 12-18).

As per claim 6, Huang et al teach the claimed command multiplier that generates multiple sets of command, address, and data inputs (CAD) from a seed CAD set having a plurality of bits provided at a low frequency to a memory system at a high frequency, comprising: a register (delay buffer column 4 lines 19-25); an arithmetic logic unit (ALU) (producer, column 3 lines 64-67, packet builder column 4 lines 1-11, compactor column 4 lines 26-29); and a multiplexer for time-multiplexing n generated CAD sets to the memory system at a frequency n times greater than the frequency at which the seed CAD sets are received(column 4 lines 12-18).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,928,593 Halbert et al.

This patent teaches a memory component with built-in self test includes a memory array. An input/output interface is coupled to the memory array and has a loopback. A controller is provided to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from

the memory array. A compare register is also provided to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

U.S. Patent No. 5,301,156 Talley

This patent teaches a configurable self-test circuit having an incremental address register, a configurable control circuit, a write register, a signature generator, and a scanpath. The address register stores the current RAM address to be accessed and is adapted to automatically increment the RAM address by an address increment upon receiving a clock signal. The control circuit has a normal operation mode and three test modes wherein all writes, all reads or alternating writes and reads may be performed.

U.S. Patent No. 6,294,935 Ott

This patent teaches a built-in-self-test circuit aids in testing a phase locked loop circuit. The phased locked loop has a plurality of frequency multipliers. The built-in-self-test circuit includes a frequency divider and a multiplexer. The frequency divider has a plurality of divide-by-counters. For each frequency, multiplier within the plurality of frequency multipliers there is a corresponding divide-by-counter. A ratio of a multiplier for each frequency multiplier to a divider of its corresponding divide-by-counter is a constant for all frequency multipliers and corresponding divide-by-counters. When a frequency multiplier within the plurality of frequency multipliers is selected, the multiplexer selects its corresponding divide-by-counter to produce a test output clock.

U.S. Patent No. 7,032,162 Dhamankar

This patent teaches a circuit for generating coefficients of an expanded polynomial, n-roots, each respective coefficient is generated at a respective one of (n+1) coefficient storage registers at one of a first place at a right most place to a (n+1) place at a left most place. In addition, a temporary coefficient is stored as the respective coefficient that was at the first place in a prior clock cycle. Such coefficients are initialized, and then an i.sup.th order multiplier output is generated by multiplying an i.sup.th order root with the respective coefficient at the first place, and an i.sup.th order adder output is generated by adding the temporary coefficient to the i.sup.th order multiplier output. The respective coefficients at and to the right of an (i+1) place are shifted toward the right with the respective coefficient at the first place becoming the temporary coefficient. The i.sup.th order adder output then becomes the respective coefficient at the (i+1) place. Such a process is performed an (i+1) times for the i.sup.th order root with (i+1) clock cycles and for each of the n-roots, for i=1 to n, to generate the respective coefficients of the expanded polynomial.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138